Features

- **Up to 2 Gsps Sampling Rate**
- **Power Consumption: 4.6W**
- **500 mVpp Differential 100Ω or Single-ended 50Ω (±2 %) Analog Inputs**
- **Differential 100Ω or Single-ended 50Ω Clock Inputs**
- **ECL or LVDS Output Compatibility**
- **50Ω Differential Outputs with Common Mode not Dependent on Temperature**
- **ADC Gain Adjust**
- **Sampling Delay Adjust**
- **Offset Control Capability**
- **Data Ready Output with Asynchronous Reset**
- **Out-of-range Output Bit**
- **Selectable Decimation by 32-function**
- **Gray or Binary Selectable Output Data; NRZ Output Mode**
- **Pattern Generator Output (for Acquisition System Monitoring)**
- **Radiation Tolerance Oriented Design (More Than 100 Krad (Si) Expected)**
- **CI-CGA152 Cavity Down Hermetic Package**
- **CBGA 152 Package Evaluation Board TSEV83102G0BGL**
- **Companion Device: DMUX 8-/10-bit 1:4/1:8 2 Gsps TS81102G0**

Performance

- 3.3 GHz Full Power Input Bandwidth (-3 dB)
- Gain Flatness: ± 0.2 dB (from DC up to 1.5 GHz)
- Low Input VSWR: 1.2 Max from DC to 2.5 GHz
- SFDR = -59 dBc; 7.6 Effective Bits at F_S = 1.4 Gsps, F_{IN} = 700 MHz [-1 dBFS]
- SFDR = -53 dBc; 7.1 Effective Bits at Fs = 1.4 Gsps, F_{IN} = 1950 MHz [-1 dBFS]
- SFDR = -54 dBc; 6.5 Effective Bits at F_S = 2 Gsps, F_{IN} = 2 GHz [-1 dBFS]
- Low Bit Error Rate (10^{-12}) at 2 Gsps

Application

- Direct RF Down Conversion
- Wide Band Satellite Receiver
- High-speed Instrumentation
- High-speed Acquisition Systems
- High-energy Physics
- Automatic Test Equipment
- Radar

Screening

- Temperature Range for Packaged Device:
  - "M" Grade: -40° C < T_C; T_J < 125° C
- Standard Die Flow (upon Request)

Description

The TS83102G0BMGS is a monolithic 10-bit analog-to-digital converter, designed for digitizing wide bandwidth analog signals at very high sampling rates of up to 2 Gsps. It uses an innovative architecture, including an on-chip Sample and Hold (S/H). The 3.3 GHz full power input bandwidth and band flatness performances enable the digitizing of high IF and large bandwidth signals.

10-bit 2 Gsps ADC MIL

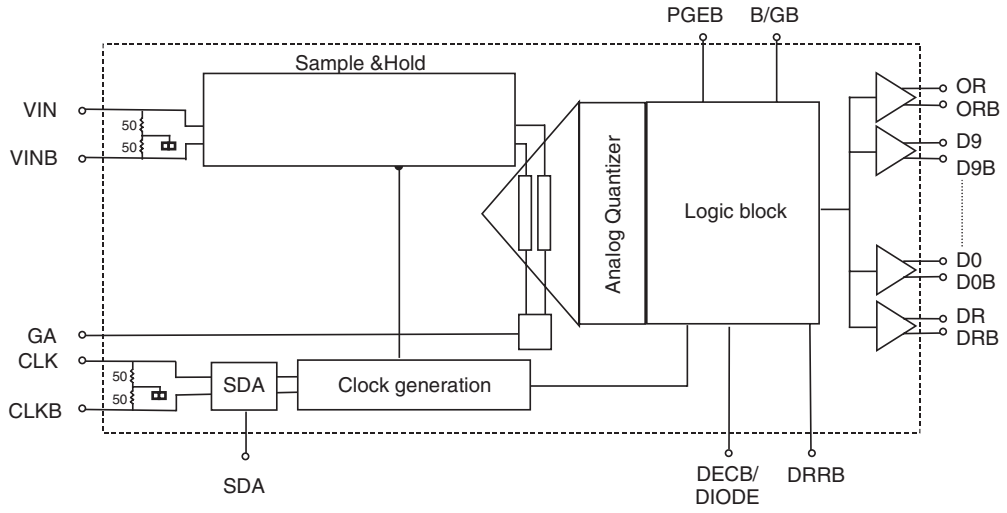
TS83102G0BMGS

Summary

For more information, please contact
hotline-bdc@gfo.atmel.com

5360AS–BDC–08/04

Figure 1. Simplified Block Diagram



Functional Description

The TS83102G0BMGS is a 10-bit 2 Gsps ADC. The device includes a front-end master/slave Track and Hold stage (Sample and Hold), followed by an analog encoding stage (Analog Quantizer), which outputs analog residues resulting from analog quantization. Successive banks of latches regenerate the analog residues into logical levels before entering an error correction circuit and resynchronization stage, followed by 50Ω differential output buffers.

The TS83102G0BMGS works in a fully differential mode from analog inputs to digital outputs. A differential Data Ready output (DR/DRB) is available to indicate when the outputs are valid and an Asynchronous Data Ready Reset ensures that the first digitized data corresponds to the first acquisition.

The control pin B/GB (A11 of the CI-CGA package) is provided to select either a binary or gray data output format. The gain control pin GA (R9 of the CI-CGA package) is provided to adjust the ADC gain transfer function.

A Sampling Delay Adjust function (SDA) may be used to ease the interleaving of ADCs.

A pattern generator is integrated on the chip for debug or acquisition setup. This function is activated through the PGEB pin (A9 of the CI-CGA package).

An Out-of-range bit (OR/ORB) indicates when the input overrides 0.5 Vpp.

A selectable decimation by 32 functions is also available for enhanced testability coverage (A10 of the CI-CGA package), along with the die junction temperature monitoring function.

The TS83102G0BMGS uses only vertical isolated NPN transistors together with oxide isolated polysilicon resistors, which provides enhanced radiation tolerance (over 100 kRad (Si) total dose expected tolerance).

TS83102G0BMGS Package Description

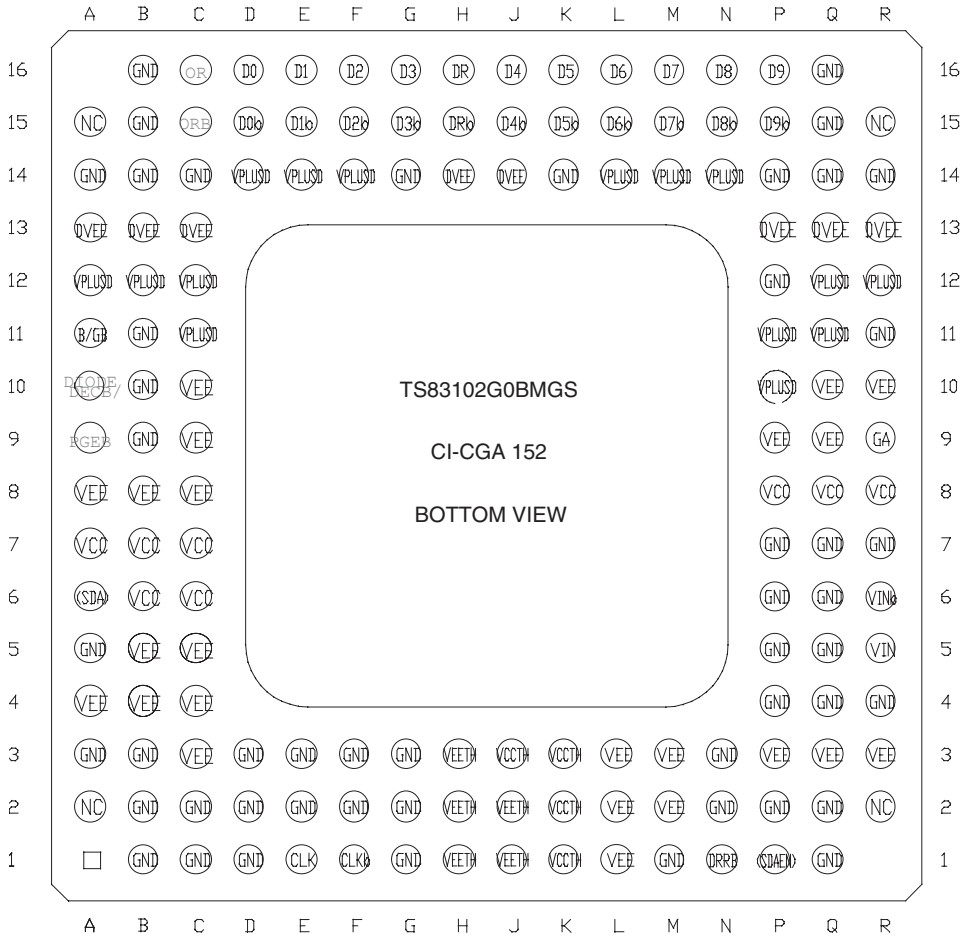
Table 1. Pin Description (CI-CGA 152)

Symbol	Pin Number	Function
Power Supplies		
V_{CC}, V_{CCTH}	K1, K2, J3, K3, B6, C6, A7, B7, C7, P8, Q8, R8	5V analog supply (connected to same power supply plane)
GND	B1, C1, D1, G1, M1, Q1, B2, C2, D2, E2, F2, G2, N2, P2, Q2, A3, B3, D3, E3, F3, G3, N3, P4, Q4, R4, A5, P5, Q5, P6, Q6, P7, Q7, R7, B9, B10, B11, R11, P12, A14, B14, C14, G14, K14, P14, Q14, R14, B15, Q15, B16, Q16	Analog ground
V_{EE}, V_{EETH}	H1, J1, L1, H2, J2, L2, M2, C3, H3, L3, M3, P3, Q3, R3, A4, B4, C4, B5, C5, A8, B8, C8, C9, P9, Q9, C10, Q10, R10	-5V analog supply (connected to same power supply plane)
V_{PLUSD}	P10, C11, P11, Q11, A12, B12, C12, Q12, R12, D14, E14, F14, L14, M14, N14	Digital positive supply
DV_{EE}	A13, B13, C13, P13, Q13, R13, H14, J14	-5V digital supply
Analog Inputs		
VIN	R5	In-phase (+) analog input signal of the differential Sample & Hold preamplifier
VINB	R6	Inverted phase (-) analog input signal of the differential Sample & Hold preamplifier
Clock Inputs		
CLK	E1	In-phase (+) clock input
CLKB	F1	Inverted phase (-) clock input
Digital Outputs		
D0, D1, D2, D3, D4, D5, D6, D7, D8, D9	D16, E16, F16, G16, J16, K16, L16, M16, N16, P16	In-phase (+) digital outputs D0 is the LSB, D7 is the MSB
D0B, D1B, D2B, D3B, D4B, D5B, D6B, D7B, D8B, D9B	D15, E15, F15, G15, J15, K15, L15, M15, N15, P15	Inverted phase (-) digital outputs
OR	C16	In-phase (+) out-of-range output
ORB	C15	Inverted phase (-) out-of-range output
DR	H16	In-phase (+) data ready signal output
DRB	H15	Inverted phase (-) data ready signal output
Additional Functions		
B/GB	A11	Binary or gray select output format control - Binary output format if B/GB is floating or connected to GND - Gray output format if B/GB is connected to V_{EE}

Table 1. Pin Description (CI-CGA 152) (Continued)

Symbol	Pin Number	Function
DECB/DIODE	A10	Decimation function enable or die junction temperature measurement: - Decimation active when LOW (die junction temperature monitoring is not possible) - Normal mode when HIGH or left floating - Die junction temperature monitoring when current is applied
PGEB	A9	Active low pattern generator enable - Digitized input delivered at outputs according to B/GB if PGEB is floating or connected to GND - Checker board pattern delivered at outputs if PGEB is connected to V_{EE}
DRRB	N1	Asynchronous data ready reset function (active at ECL low level)
GA	R9	Gain adjust
SDA	A6	Sampling delay adjust
SDAEN	P1	Sampling delay adjust enable - Inactive if floating or connected to GND - Active if connected to V_{EE}

Figure 2. Pinout



Notes: 1. To simplify PCB routing, the 4 NC columns can be electrically connected to the GND columns.
2. The pinout is shown from the bottom. The columns and rows are defined differently from the JEDEC standard.

Thermal and Moisture Characteristics

Dissipation by Conduction and Convection

The thermal resistance from junction to ambient RTH_{JA} is around 30° C/W. Therefore, to lower RTH_{JA}, it is mandatory to use an external heat sink to improve dissipation by convection and conduction. The heat sink should be fixed in contact with the top side of the package (Al203 electrical isolation over CuW heat spreader).

The heat sink does not need to be electrically isolated, because the top of the package is already electrically isolated thanks to a 0.30 mm Al203 layer.

Example:

The thermal resistance from case to ambient RTH_{CA} is typically 4.0° C/W (0 m/s air flow or still air) with the heat sink depicted in Figure 3 on page 7, of dimensions 50 mm x 50 mm x 28 mm (respectively L x l x H).

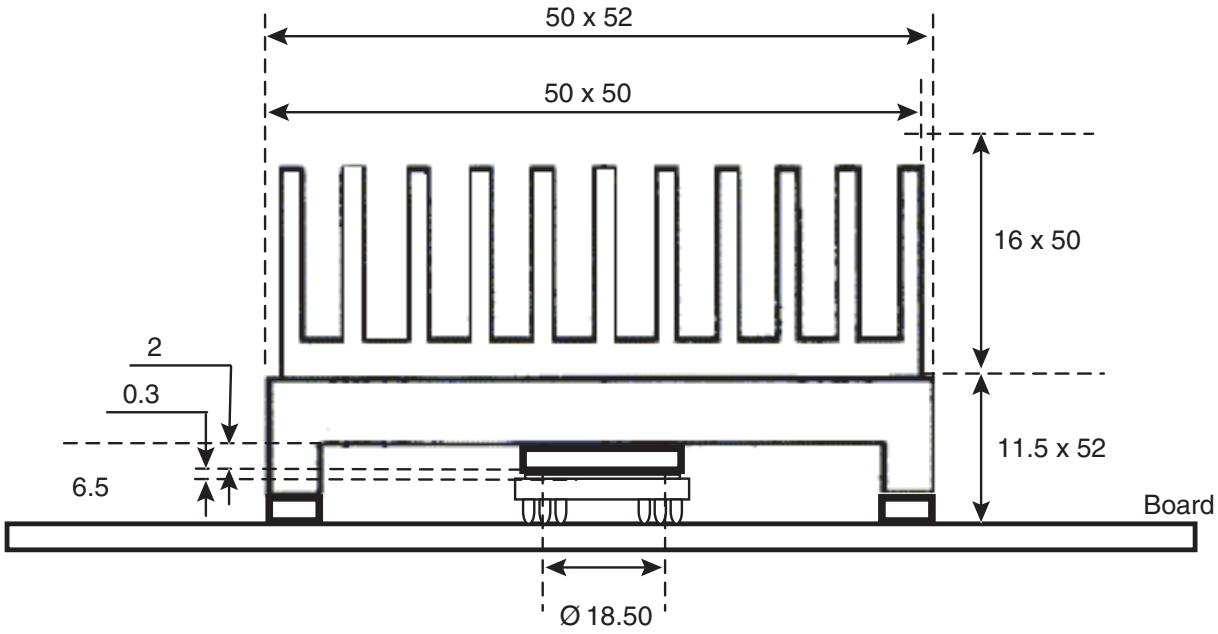
The global junction to ambient thermal resistance RTH_{JA} is:
4.8° C/W RTH_{JC} + 2.0° C/W thermal grease resistance + 4.0° C/W RTH_{CA} (case to ambient) = 10.8° C/W total (RTH_{JA}).

Assuming:

A typical thermal resistance from the junction to the top of the case RTH_{JC} of 4.8° C/W (finite element method thermal simulation results): this value does not include the thermal contact resistance between the package and the external heat sink (glue, paste, or thermal foil interface, for example). As an example, use a 2.0° C/W value for a 50 µm thickness of thermal grease.

Note: Example of the calculation of the ambient temperature T_A max to ensure T_J max = 110° C: assuming RTH_{JA} = 10.8° C/W and power dissipation = 4.6 W, T_A max = T_J - (RTH_{JA} x 4.6 W) = 110 - (10.8 x 4.6) = 60.32° C. T_A max can be increased by lowering RTH_{JA} with an adequate air flow (2 m/s, for example).

Figure 3. Black Anodized Aluminium Heat Sink Glued on a Copper Base Screwed on Board (all dimensions in mm)



Note: The cooling system efficiency can be monitored using the temperature sensing diodes integrated in the device.

Thermal Dissipation by Conduction Only

When the external heat sink cannot be used, the relevant thermal resistance is the thermal resistance from the junction to the bottom of the columns: $RTH_{J\text{-}Bottom\text{-}of\text{-}columns}$.

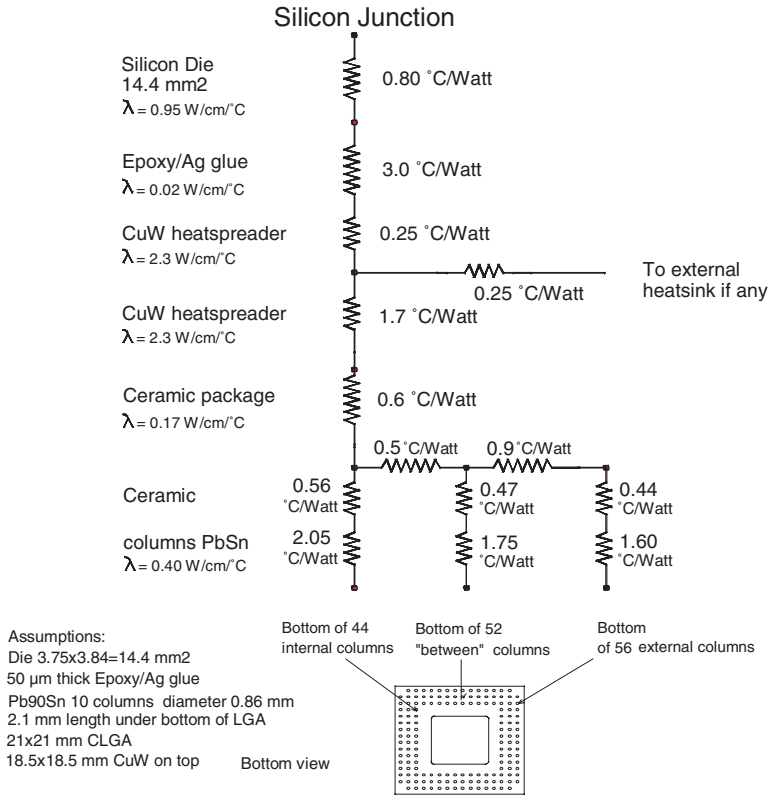
The thermal path, in this case, is the junction, then the silicon, glue, CuW heat spreader, package Al2O3, and the columns (Sn10Pb90).

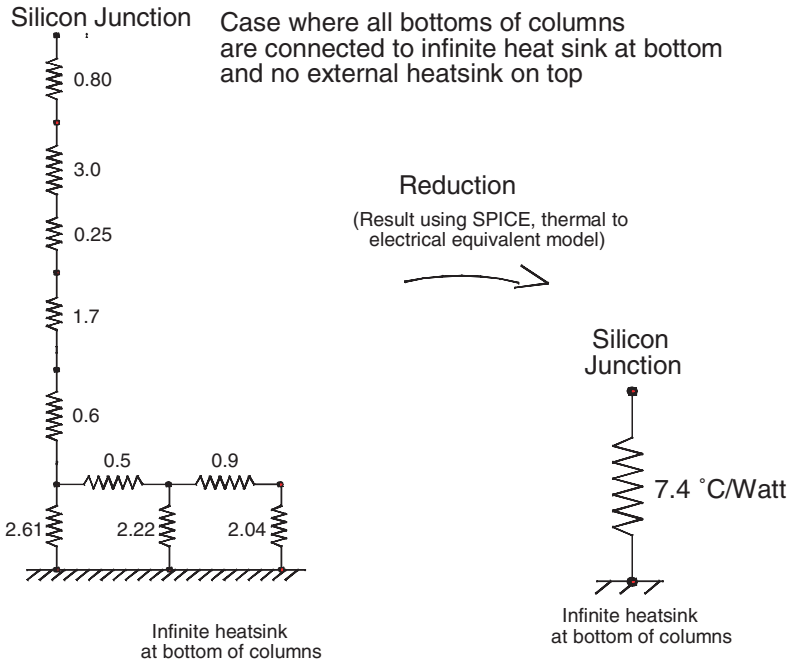
The Finite Element Method (FEM) with the thermal simulator leads to $RTH_{J\text{-}bottom\text{-}of\text{-}columns} = 7.4°C/W$. This value assumes pure conduction from the junction to the bottom of the columns (this is the worst case, no radiation and no convection is applied). With such an assumption, $RTH_{J\text{-}\ Bottom\text{-}of\text{-}columns}$ is user-independent.

To complete the thermal analysis, you must add the thermal resistance from the top of the board (on which the device is soldered) to the ambient resistance, whose values are user-dependent (the type of board, thermal, routing, area covered by copper in each board layer, thickness, airflow or cold plate are all parameters to consider).

In the case of the CI-CGA 152 package, the thermal resistance from the junction to the top of the package (via the CuW heat spreader covered by AI203) is $RTH_{J\text{-}top\text{-}of\text{-}package} = 4.8°C/W$.

Figure 4. Thermal Net

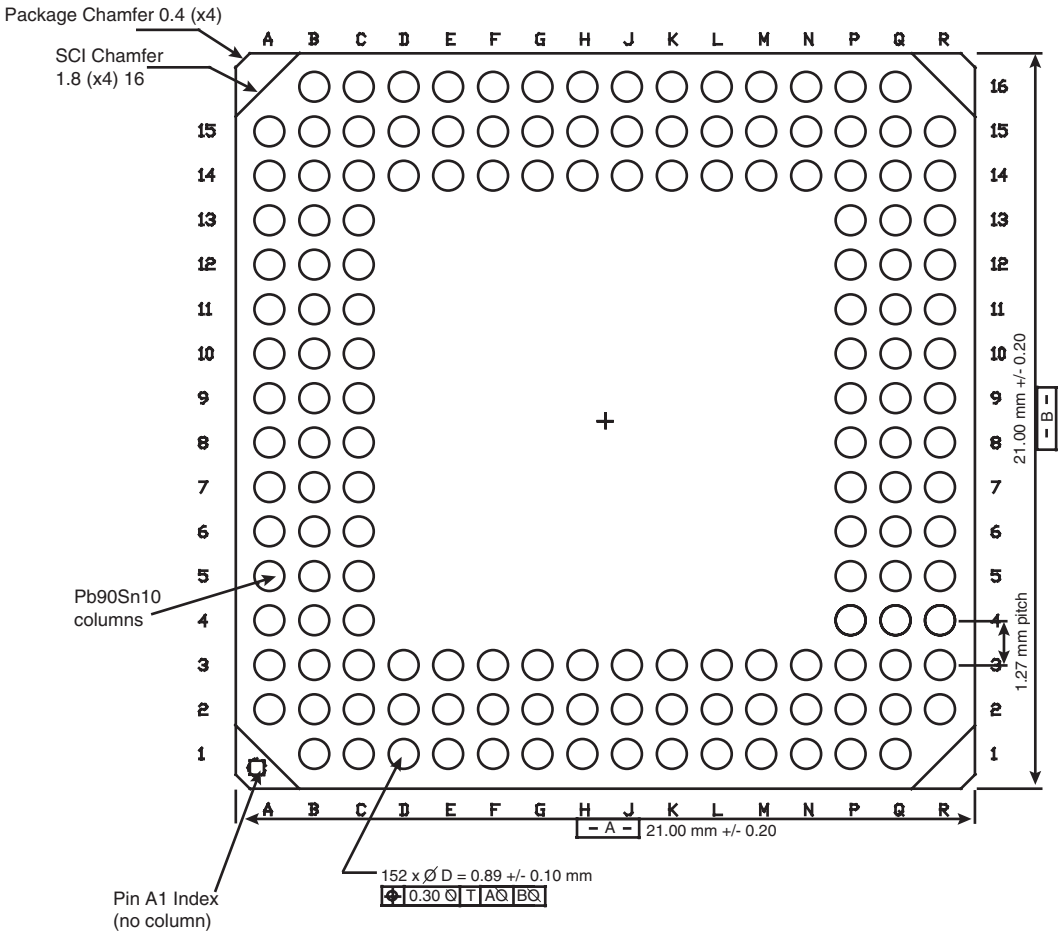




Package Description

Hermetic CI-CGA 152 Outline Dimensions

Figure 5. Mechanical Description Bottom View



Note: CuW Heat Spreader on Opposite Side of Package

Ceramic body size : 21 x 21 mm

Column pitch : 1.27 mm

Cofired : Al2O3

Figure 6. Package Top View

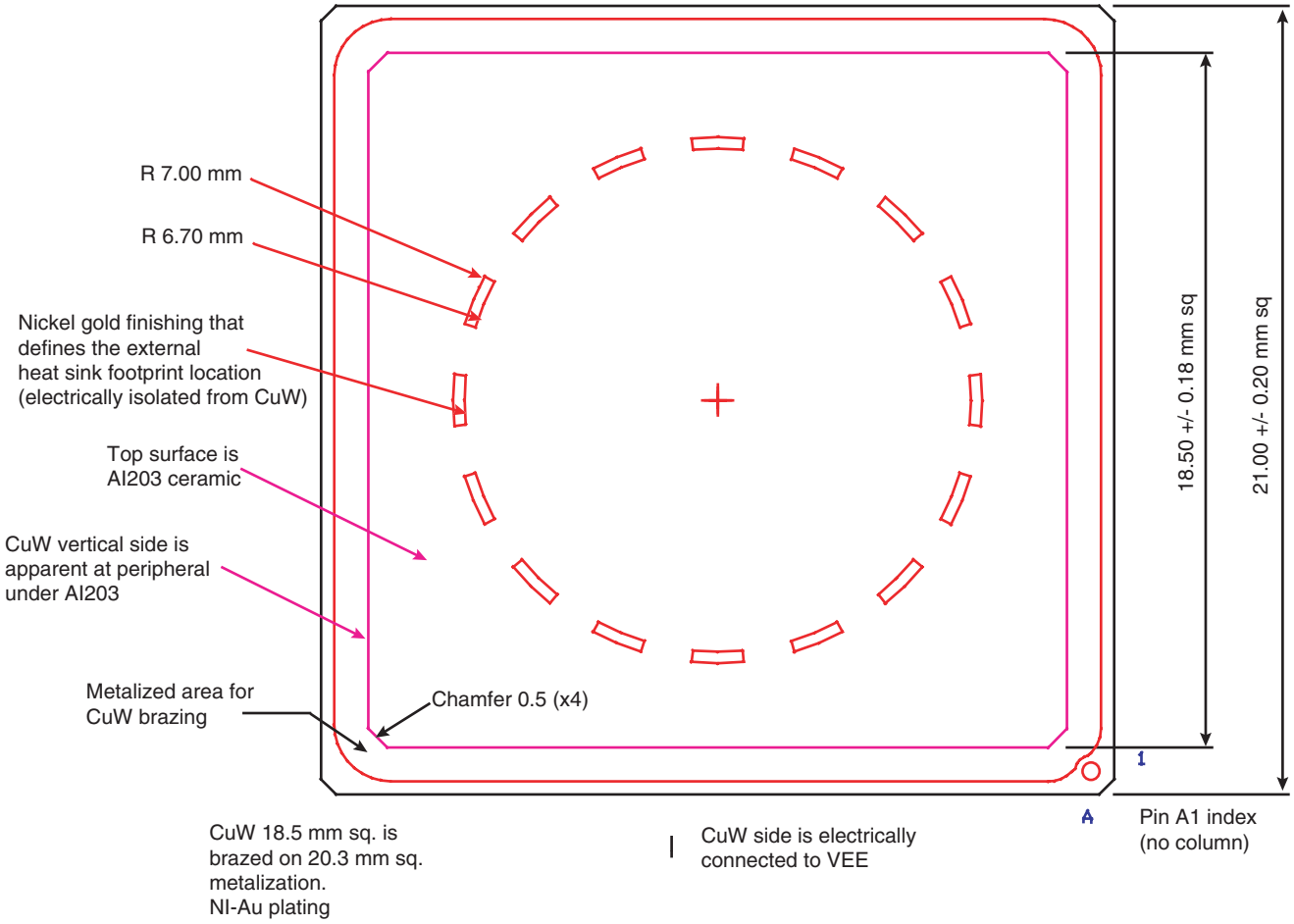
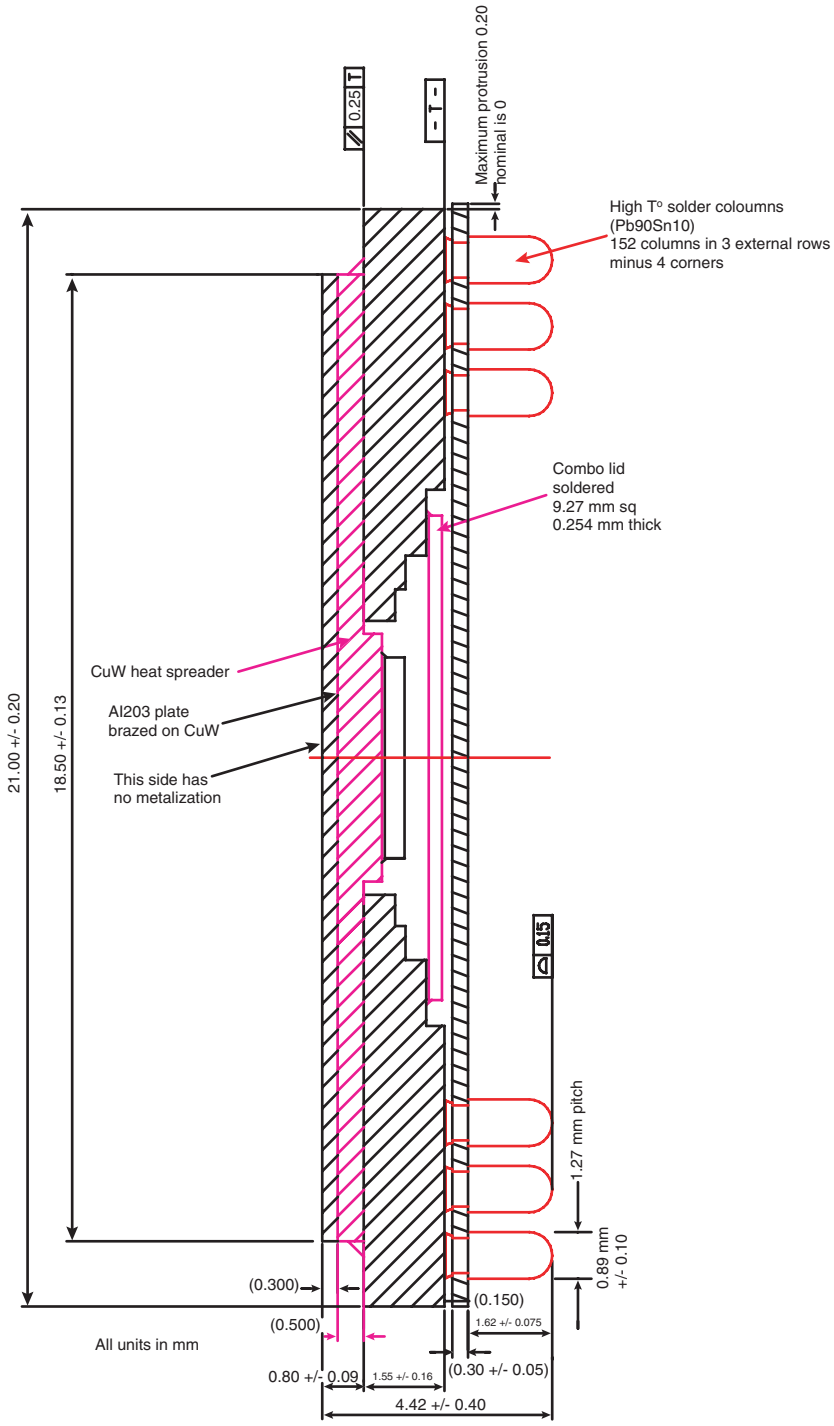


Figure 7. Cross Section



Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
TSX83102G0BGS	CI-CGA152	Ambient	Prototype	Please contact your local Atmel sales office
TS83102G0BMGS	CI-CGA 152	-40° C < T_c; T_J < 125° C	Standard product	
TSEV83102G0BGL	CBGA 152	Ambient	Prototype	Evaluation Board (delivered with a heat sink)

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